We Claim:

1. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a surface with a conductive layer thereon; and

laser machining a plurality of grooves through the conductive layer to the surface, the grooves defining a plurality of conductors on the surface, each conductor comprising a portion of the conductive layer with a groove on either side thereof.

2. The method of claim 1 further comprising forming a plurality of conductive vias in the substrate in electrical communication with the conductors.

3. The method of claim 2 further comprising forming an array of contact balls on an opposing second surface of the substrate in electrical communication with the conductive vias and conductors.

4. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a first surface and an opposing second surface, the first surface having a conductive layer thereon;

laser machining a plurality of grooves through the conductive layer to the surface, the grooves defining a plurality of conductors on the surface, each conductor comprising a portion of the conductive layer with a groove on either side thereof;

forming a plurality of conductive vias in the substrate in electrical communication with the conductors, each

conductive via extending from the first surface to the second surface; and

forming a plurality of contact balls on the second surface in electrical communication with the conductive vias.

5. The method of claim 4 further comprising mounting a semiconductor die to the first surface in electrical communication with the conductors.

6. The method of claim 4 wherein the substrate comprises silicon.

7. The method of claim 4 wherein forming the conductive vias comprises laser machining openings in the substrate and depositing a conductive material within the openings.

8. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a surface with a conductive layer thereon;

laser machining a plurality of grooves through the conductive layer to the surface, the grooves defining a plurality of conductors on the surface, each conductor comprising a portion of the conductive layer with a groove on either side thereof;

laser machining a plurality of pads on the surface in electrical communication with the conductors; and

mounting a semiconductor die to the surface in electrical communication with the pads.

9. The method of claim 8 wherein the mounting step comprised wire bonding bond pads on the semiconductor die to the pads.

10. The method of claim 8 wherein the mounting step comprises flip chip mounting the semiconductor die to the pads.

11. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a surface with a conductive layer thereon, the conductive layer having a thickness; and

laser machining a plurality of grooves through the conductive layer to the surface, the grooves defining a first conductor and a second conductor on the surface, the first conductor comprising a signal path for the component, the second conductor in electrical communication with a ground or voltage path, with the thickness of the conductive layer and a width of the grooves selected to provide an impedance value for the first conductor.

12. The method of claim 11 wherein the component comprises a multi chip module.

13. The method of claim 11 wherein the component comprises a chip scale package.

14. The method of claim 11 wherein the component comprises a test carrier for testing a second semiconductor component.

15. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a surface with a conductive layer thereon, the conductive layer having a thickness;

laser machining a plurality of conductors in the conductive layer, each conductor defined by a pair of grooves through the conductive layer, the conductors including a plurality of first pads;

mounting a semiconductor die to the substrate, the die comprising a plurality second pads bonded to the first pads; and

selecting the thickness of the conductive layer, and a width of the grooves, to provide an impedance for the conductors.

16. The method of claim 15 further comprising forming a plurality of external contacts on the substrate in electrical communication with the conductors.

17. The method of claim 16 wherein the external contacts comprise balls in a ball grid array.

18. The method of claim of claim 17 further comprising forming conductive vias through the substrate in electrical communication with the conductors and with the external contacts.

19. The method of claim 18 wherein forming the conductive vias comprises laser machining openings in the substrate and filling the openings with a conductive material.

20. The method of claim 19 wherein the substrate comprises silicon.

21. A method for fabricating a semiconductor component comprising:

providing a substrate comprising a first surface and an opposing second surface, the first surface having a conductive layer thereon;

laser machining a plurality of grooves through the conductive layer to the first surface, the grooves defining a plurality of conductors on the first surface, each conductor comprising a portion of the conductive layer with a groove on either side thereof, each conductor comprising a pad;

forming a plurality of conductive vias in the substrate in electrical communication with the conductors, each conductive via extending from the first surface to the second surface;

forming a plurality of external contacts on the second surface in electrical communication with the conductive vias; and

mounting a semiconductor die to the first surface in electrical communication with the conductors.

22. The method of claim 21 further comprising encapsulating the die by depositing an encapsulant on the first surface.

23. The method of claim 21 wherein the external contacts comprise balls in a ball grid array.

24. The method of claim 21 wherein the component comprises a chip scale package.

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25. A semiconductor component comprising;

a substrate comprising a first surface with a conductive layer thereon, and a second surface;

a plurality of conductors on the first surface, each conductor comprising at least one laser machined groove

through the conductive layer, each conductor configured for electrical communication with a semiconductor die;

a plurality of conductive vias in the substrate in electrical communication with the conductors; and

a plurality of external contacts on the second surface in electrical communication with the conductive vias.

26. The component of claim 25 further comprising a plurality of semiconductor dice wire bonded to the conductors.

27. The component of claim 25 further comprising a plurality of semiconductor die flip chip mounted to the conductors.

28. The component of claim 25 wherein the substrate comprises a material selected from the class consisting of plastic, glass filled resin, silicon and ceramic.

29. The component of claim 25 wherein the external contacts comprise balls in a ball grid array.

30. A semiconductor component comprising;

a substrate comprising a surface with a conductive layer thereon having a thickness; and

a plurality of conductors on the surface, the conductors comprising laser machined grooves through the conductive layer, the conductors including a first conductor configured as a signal path for the component and a second conductor in electrical communication with a ground or voltage path, with the thickness of the conductive layer and a width of the grooves selected to provide an impedance value for the first conductor.

31. The component of claim 30 further comprising a plurality of external contacts on the substrate in electrical communication with the conductors.

32. The component of claim 31 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors and with a plurality of external contacts formed on a second surface of the substrate.

33. The component of claim 32 further comprising a semiconductor die mounted to the substrate in electrical communication with the conductors.

34. The component of claim 33 further comprising an encapuslant covering the die and at least a portion of the surface.

35. A semiconductor component comprising:

a substrate comprising a surface with a conductive layer thereon, the conductive layer having a thickness;

a plurality of laser machined conductors in the conductive layer, each conductor defined by a pair of grooves through the conductive layer, the conductors including a plurality of first pads;

a semiconductor die mounted to the substrate, the die comprising a plurality second pads bonded to the first pads; and

with the thickness of the conductive layer, and a width of the grooves selected to provide an impedance for the conductors.

36. The component of claim 35 further comprising an encapsulant covering the die and at least a portion of the surface.

37. The component of claim 35 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors and with a plurality of contact balls formed on a second surface of the substrate.

38. The component of claim 35 wherein the substrate comprises silicon with an insulating layer on the surface.

39. The component of claim 35 wherein the substrate comprises a material selected from the class consisting of plastic, glass filled resin and ceramic.

40. A test carrier for a semiconductor component comprising:

a base comprising a surface with a conductive layer thereon;

a plurality of conductors on the first surface, each conductor comprising at least one laser machined groove through the conductive layer; and

an interconnect mounted to the surface, the interconnect comprising a plurality of first contacts in electrical communication with the conductors and configured for electrical connection to a plurality of second contacts on the component.

41. The test carrier of claim 40 further comprising a plurality of conductive vias in the base in electrical communication with the conductors and with a plurality of external contacts formed on a second surface of the base and configured for electrical communication with test circuitry.

42. The test carrier of claim 40 further comprising a force applying mechanism attached to the base for biasing the component against the interconnect.

43. A test carrier for a semiconductor component comprising:

a base comprising a surface with a conductive layer thereon having a thickness;

a plurality of conductors on the first surface, each conductor comprising at least one laser machined groove through the conductive layer; and

an interconnect mounted to the surface, the interconnect comprising a plurality of first contacts in electrical communication with the conductors and configured for electrical connection to a plurality of second contacts on the component;

with the thickness of the conductive layer, and a width of the grooves selected to provide an impedance for the conductors.

44. The test carrier of claim 43 further comprising a plurality of conductive vias in the base in electrical communication with the conductors and with a plurality of balls on a second surface of the base in a ball grid array.

45. The test carrier of claim 43 wherein the semiconductor component comprises an unpackaged die.

46. The test carrier of claim 43 wherein the semiconductor component comprises a chip scale package.

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